**EXPERIMENT#1**

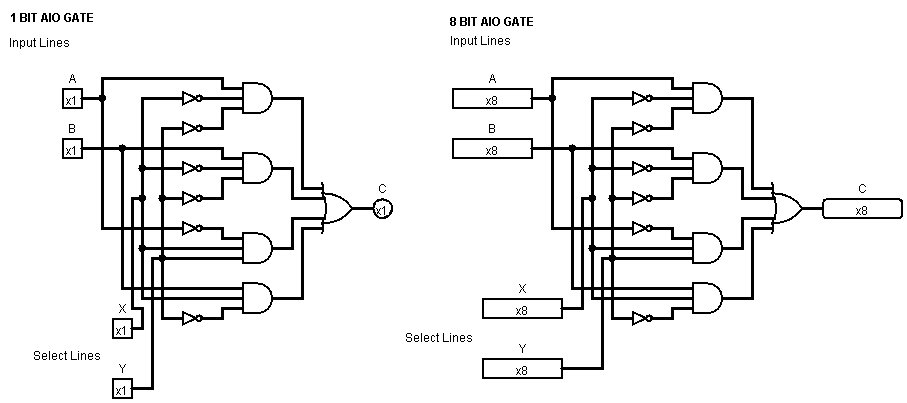
**Aim: Designing of basic digital circuits using logic gates.**

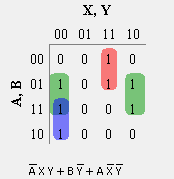
**Exercise#1:** Design two inputs and five outputs All-in-One logic gate circuit shown in Fig.1 using Logisim simulator with (i) data width 1 (ii) data width 4.

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| C = not A  D = A.B  E = A+B  F = ~(A.B)  G = AB |  |
| **Truth Table or Karnaugh (K) Map** |
|  |

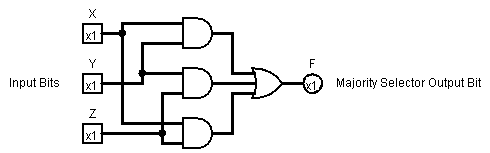
**Exercise#2:** Design two inputs and one output All-in-One logic gate diagram shown in Fig.2 using Logisim simulator with (i) data width 1 (ii) data width 8.

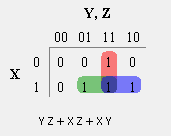
**Logic Diagram :**



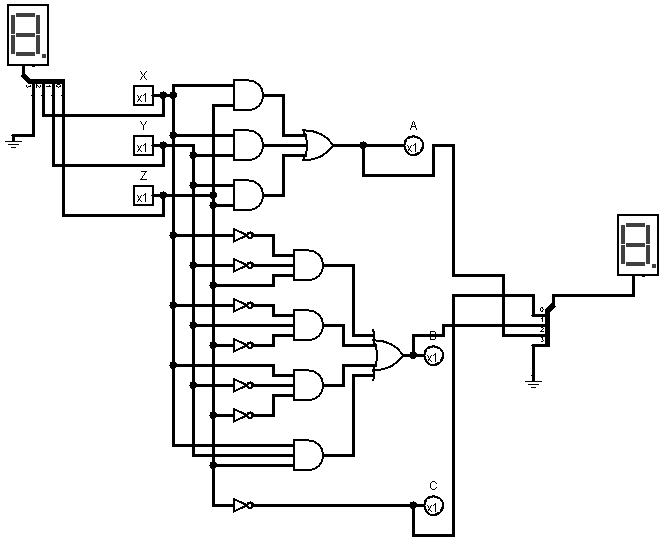
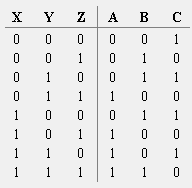
**Boolean expression and K-Map :**

**Exercise#3:** Design a three-input majority detector combinational digital circuit using Logisim simulator which shows output equal to 1 if the input variables have more 1's than 0's, the output is 0 otherwise.

**Logic Diagram: Boolean Expression and K-Map:**

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**Exercise#4:** Design a combinational circuit with three inputs and three outputs. When the input is 0, 1, 2, or 3, the output is one greater than the input and when the input is 4, 5, 6, or 7, the output is one less than the input. Display the input and output digits using Hex digit display with splitter.

**Logic Diagram:**  **Boolean Expressions & Truth Table :**

A= Y Z + X Z + X Y

B= ~X ~Y Z + ~X Y ~Z + X ~Y ~Z + X Y Z

C= ~Z